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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,722	12/16/2003	Ki Chon Park	29936/39878	3556

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,722	PARK, KI CHON	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 and 16* is/are allowed.

6)☒ Claim(s) *1,2,4,13,14 and 17-19* is/are rejected.

7)☒ Claim(s) *3,5,6,8-12,20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 4/15/2005 has been reviewed and considered with the following results:

As to the objections to the specification, Applicant's amendments have overcome the objections, as such; the objections have been withdrawn.

As to the rejection to the claims, under 35 U.S.C. 112, 2nd paragraph, Applicant's amendments of the claims have overcome the rejections, as such; the rejections have been withdrawn.

As to the prior art rejections to the claims made in the previous Office Action are now withdrawn in view of Applicant's amendments. However, Applicant's amendments necessitate new ground of rejection as set forth below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4, 13, 14, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (US Pat. 5,844,438; previously cited).

With regard to claims 1 and 14, Lee discloses in Figs. 2-7 a circuit, and a method of use thereof, for generating an internal clock signal, comprising an operating frequency decision unit

(50, 80) for determining whether an external clock signal (CLK) is a low frequency or a high frequency depending on a column address strobe latency (ref-oh; by given the broadest reasonable interpretation the signal **ref-oh** can be seen as the column address strobe latency) and outputting a detecting signal (/OUT); and an internal clock signal generator (60, 70) for waveform-shaping the external clock signal and generating the internal clock signal (CLKDQ) depending on an output of the operating frequency decision unit (/OUT).

With regard to claim 2, the operating frequency decision unit comprises an inverter (81) for inverting a level of a most significant bit of the column address strobe latency (by given the broadest reasonable interpretation the signal SS can be seen as the most significant bit).

With regard to claim 4, the circuit further comprises a mode register (55, 56) for storing the CAS latency.

With regard to claim 13, the internal clock signal has the same pulse width as that of the external clock signal or has the pulse width corresponding to delay time of the delay unit (61, 71, 74).

Claims 18 and 19 are similarly rejected; note the above discussion with regard to claims 1, 2, and 14.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee.

Claim 17 is similarly rejected; note the above discussion with regard to claims 1 and 14. Furthermore, the limitation that "generating the external clock signal as the internal clock signal as it is if the external clock signal is the high frequency" is also very obvious. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to either implement the internal clock signal generator (70) for waveform-shaping the external clock signal; or not using the internal clock signal generator by but rather using the external clock signal as the internal clock signal, which are in each case optimally matched to its application.

Allowable Subject Matter

6. Claims 3, 5, 6, 8-12, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 7 and 16 are allowed.

The prior art of record fails to disclose or fairly suggest circuit for generating an internal clock signal (as shown in Fig. 3) and a method of use thereof, as recited in claims 3 and 16, having specific structural limitations such as the CAS latency has a value of 0 to 7 and the operating frequency decision unit (310 in instant Fig. 4) generates the detecting signal (HF) if the value of the CAS latency is over 4, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest circuit for generating an internal clock signal (as shown in Fig. 3) and a method of use thereof, as recited in claims 5, having specific structural limitations such as an internal clock signal generator (320 in instant Fig. 3) comprises a delay unit (D320) for delaying the external clock signal (Ext_CLK) by some time; and a pulse-shaping unit (P330) for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the output (HF) of the operating frequency decision unit (310), or generating the external clock signal as the internal clock signal (Int_CLK) as it is, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a circuit for generating an internal clock signal, as recited in claim 7, having specific structural limitation such as a pulse-shaping unit (P320 in instant Fig. 3) for logically combining the external clock signal (Ext_CLK) with the output of the delay unit and generating the internal clock signal (Int_CLK) depending on the output detecting signal (HF) of the operating frequency decision unit (310), or generating the external clock signal as the internal clock signal as it is, the pulse-shaping unit comprising a first NAND gate (N321) for logically combining the external clock signal (Ext_CLK) with the output signal of the delay unit (A) depending on the detecting signal (HF) of the operating frequency decision unit; a second NAND gate (N322) into which the external clock signal and the output signal of the first NAND gate are inputted; and an inverter (I321) for inverting the output signal of the second NAND gate; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

Claim 20 is allowed for similar reasons; note the above discussion with regard to claim 7.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
July 10, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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